P-*InAsSbP*/n-*InAs* single heterostructure back-side illuminated 8 × 8 photodiode array

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HIGHLIGHTS

- BLIP regime starting from 190 K at 3 μm.
- Capacitance as small as 1.3×10^{-7} F cm^{-2}, 80 K.
- Good uniformity of diode parameters in 8 × 8 PD matrix.

ARTICLE INFO

ABSTRACT

P-*InAsSbP*/n-*InAs*/n$^+$-*InAs* single heterostructure photodiode monolithic array with linear impurity distribution in the space charge region and "bulk" n-InAs absorbing layer has been fabricated by the LPE method and studied for the first time. Unlike all known InAsSbP/InAs PDs with an abrupt p-n junction the linear impurity distribution PDs potentially suggest lower compared with analogs capacitance and tunneling current. Indeed the developed photodiodes showed good perspectives for use in low temperature pyrometry as low dark current (8×10^{-6} A/cm^2, $U_{bias} = -0.5$ V, 164 K) and background limited infrared photodetector (BLIP) regime starting from 190 K (2π field of view, $D^*_{3.1\ \mu m} = 1.1 \times 10^{12}$ cm Hz$^{1/2}$/W) have been demonstrated. High photodiode performance is thought to be due to above peculiarities of the impurity distribution as well as low defect density in P-*InAsSbP*/n-*InAs*/n$^+$-*InAs* single heterostructure.

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1. Introduction

InAsSbP/InAs based photodiodes (PDs) are used in low temperature pyrometry [1,2], nondispersive infrared (NDIR) analysis of hydrocarbon gases [3] and thermophotovoltaics [4]. However, performance of most known *InAsSbP/InAs* based PDs suffered from deep nonradiative Shockley-Read centers (or "structure defects") as followed e.g. from superlinear light-current (L-I) characteristic [5] and from dependence of the zero bias capacitance C_o on a modulation frequency [6]. Besides for about a decade researchers have been considering InAsSbP/InAs heterostructure diodes with an abrupt p-n junction. The latter feature was the reason for narrow space charge region which was not optimal for low capacitance/high speed operation. Recently back-side illuminated (BSI)

InAsSbP/InAs double heterostructure (DH) single element PDs with smooth impurity concentration distribution near a p-n junction (here: linear n(x)) have been fabricated [7]. These PDs have reached BLIP operation at 150 K and showed lowest among analogs capacitance. On the other hand *InAsSbP/InAs* single heterostructure (SH) growth process is easier than that for the DH one and thus it may be attractive for PD fabrication in volume. However, to the best of our knowledge there have been no publications related to *InAsSbP/InAs* SH PDs with smooth p-n junction, and there were no reports on *InAsSbP/InAs* PD arrays operating in the BLIP regime.

In this paper we discuss data on electro-physical and optical characterization of the BSI P-*InAsSbP*/n-*InAs* SH PD array (8 × 8) with smooth impurity concentration distribution near a p-n junction in the 77–385 K temperature range and report on BLIP operation at temperature of 190 K.

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2. Device fabrication and measurements

Wafers were fabricated in a similar manner as in [8] and contained transparent n+-*InAs* (*Sn*) (1 0 0) substrate (n+ = (2–3) × 10^{18} cm^{-3}), 3–4 µm thick intentionally undoped narrow-gap n-*InAs* layer and finally 2–3 µm thick wide-gap P-*InAsSbP* (*Zn*) (P = (2–5) × 10^{17} cm^{-3}) cap layer. The photoluminescence (PL) spectrum measured at 77 K in a reflection mode showed strong longwave emission peak at 0.413 eV which is a common value for the undoped n°-*InAs*; PL spectrum contains also weak short-wave peak at 0.475 eV related to recombination in P-*InAsSbP* and distorted by water vapor and CO_2 absorption (see Fig. 1). Electroluminescence (EL) peaks matched the corresponding PL peaks at 77 (hv = 0.413 eV) and 300 K (hv = 0.37 eV). Room temperature (RT) EL peak value was typical for LEDs with n°-*InAs* active layer. The RT PL spectrum contained also short wave shoulder originating from recombination in P-*InAsSbP* cap layer; this part of the spectrum was also distorted by water vapor and CO_2 absorption. Fig. 1 contains additionally transparency spectra of the epitaxial layers set as a ratio of the SH and n+-InAs substrate transmission at 300 and 77 K respectively. The above spectra were certainty disturbed by minor difference of the surface quality of the SH and substrate and by the P-InAsSbP cap layer absorption impact. Thus data on n-InAs layer transparency is not fully accurate as we didn't take into account exact value of the SH reflectivity and ignored absorption in P-InAsSbP wide gap layer.

It is worth mentioning that close proximity of p-n junction and *InAsSbP*/*InAs* interface (or in other words lack of an intermediate p-type InAs layer) follows from analysis of the EL spectra and comparison with literature data on p-InAsSbP/p-InAs samples (see similar analysis and comparison in [7]). In addition to this close proximity of p-n junction and *InAsSbP*/*InAs* interface has been also already confirmed by the Atomic Force Microscopy (AFM) measurements in P-*InAsSbP*/n-*InAs* SH [8] and DH analogs fabricated by close grown procedure.

Rectangular PD chips of 2.5 × 2.65 mm size contained 64 pieces of individually addressable mesa diodes of 190 × 190 µm dimensions as shown in Fig. 2a. Broad reflective Ag-based anode onto the P-*InAsSbP* cap layer and *Cr-Au-Ni-Au* cathode onto the n+-*InAs* substrate material were formed by evaporation in vacuum. PD chips were mounted onto Si read-out plate so that back-side illumination through a 0.2 mm thick substrate without shadowing by electrical contacts has been organized; no special passivation and antireflection coatings have been implemented. Following results and recommendations in [9] prior measurements InAs SH PDs have been wet chemically etched. Fig. 2c demonstrates matrix IR image (λ = 3 µm) together with near field radiation distribution at λ = 3 µm along substrate surface. Image depicts negative luminescence (NL) in all 64 reversely biased (RB) PD elements with fill factor of about 0.64[1].

Current-voltage (I-V) and capacitance – voltage (C-V) characteristics were measured in the same way and by the same equipment as in [7]. Unlike diodes in [10] no hysteresis phenomena has been observed in I-V characteristics.

Current sensitivity value at maximum ($S_{\lambda max}$) used in this paper refers to a value measured in a 2 × 2 "etalon" matrix with cleaved edges and minimal space outside mesa/element areas. This "ethalon" matrix was cleaved from the same wafer under study and optical area was considered to be equal to that of the chip area.

3. Results and discussion

Fig. 3 presents temperature dependent I-V characteristics for one of the best matrix elements. Values of the current below

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[1] This number refers to the area occupied by all 64 elements, that is, 2 × 2 mm^2. Area at the chip edges is not taken into account.
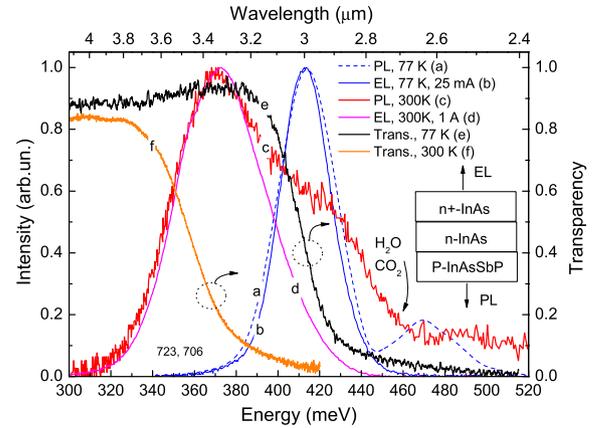
Fig. 1. Electro- and "reflection" photoluminescence spectra in InAs SH PD (a–d) together with transparency spectra at 77 and 300 K (e and f).

(a)

(b)

(c)
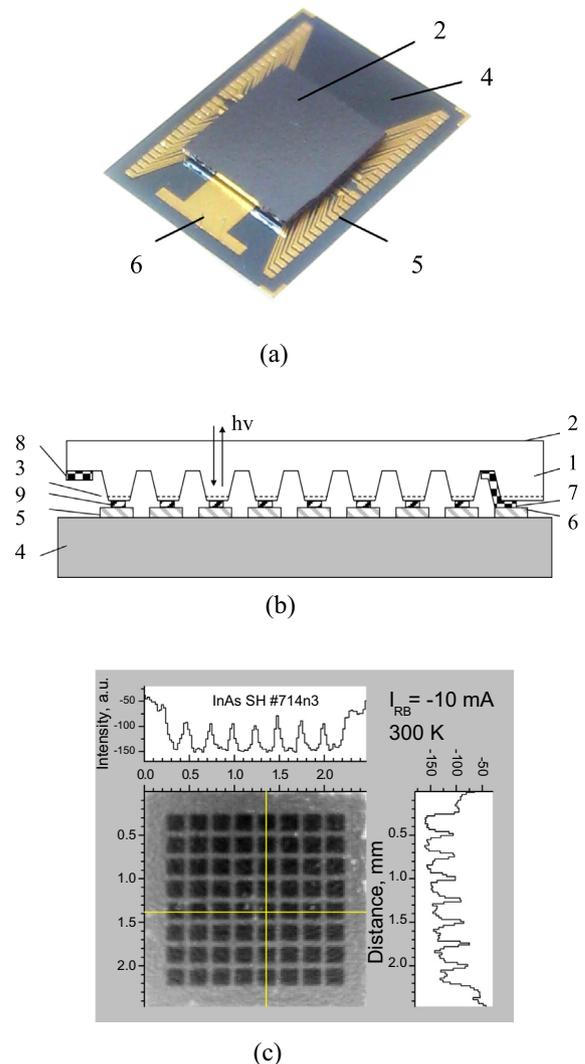
Fig. 2. General view (a), schematic (b) and IR image (c) of the BSI array (RB, I = −10 mA). 1 – P-InAsSbP/n-InAs/n+-InAs single heterostructure, 2 – n+-InAs surface, 3 – mesa walls/p-n junction, 4 – Si read-out plate, 5 – anode bonding pads, 6 – cathode bonding pad, 7 – contact to n+-InAs, 8 –ring contact to n+-InAs, 9 – contacts to individual anodes. Items 7 and 8 have short circuit. Adjacent to IR image is radiation distribution in near field along two orthogonal directions onto n+-InAs surface.
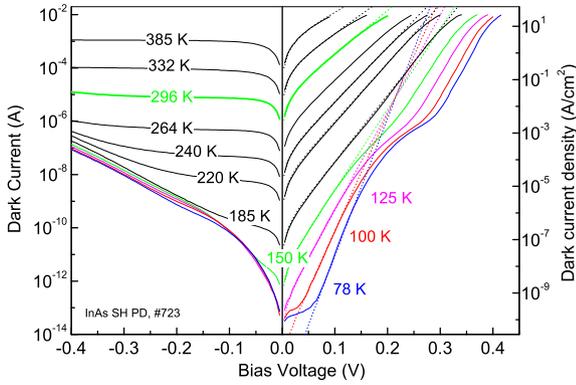
Fig. 3. Temperature-dependent semilog I-V characteristics of *InAs* SH diode.

5 × 10⁻¹⁴ A are obviously uncertain because of noise. Low temperature RB I-V characteristics (U < 0) most likely were governed by a tunnel leakage while at U ≫ 0 domination of the diffusion current was evident as the ideality factor β in the modified Shockley formula ($I = I_o[\exp(eU/\beta kT) - 1]$, where e is the electron charge, k is the Boltzmann contestant and T is the temperature) was well below 2 (see the insert in Fig. 4). At T > 160 K the zero bias resistance R_o exhibited temperature dependence that was typical for diodes with domination of the diffusion current as $R_o \sim \exp(E_a/kT)$, $E_a = E_g = 0.41$ eV (Fig. 4). At temperatures below 160 K the R_o value "saturates" probably due to tunneling; low temperature tunneling enhancement in SH PDs goes along with non-symmetrical type of I-V characteristic near zero bias and with higher than in our previous DH samples free carrier concentration near the p-n junction (see data on C-V characteristics and concentration evaluation presented below). The above "saturation" was not observed in our previous DH PDs (see the corresponding data in Fig. 4).

At RT around 70% of the inserted in heterostructure radiation at peak responsivity wavelength of 3.4 μm (300 K) is absorbed at a single pass through the narrow band InAs layer (see Fig. 1); at 77 K the above value is a little bit lower (∼57% at 3 μm). Sensitivity spectra were narrower than those for the FSI PD analogs reported previously (see e.g. [8]) due to radiation "filtering" by the n⁺-*InAs* substrate. For the same reason both $S_{\lambda max}$ and external quantum efficiency (QE) were temperature sensitive (see Fig. 5) most likely because of minority carrier diffusion length and n⁺-*InAs* transparency temperature dependence. In other words cooling dramatically enhances PD performance, e.g. external quantum efficiency grows up to 0.61 at 80 K.

Fig. 5. Peak wavelength sensitivity and external quantum efficiency vs temperature.

Figs. 6 and 7 show calculated Johnson-noise limited detectivity (D_{λ}^* and $D_{\lambda max}^*$) at several temperatures. The D^* spectrum is a little bit narrower than that for the *InAs* DH PDs [7] due to a reduction of sensitivity at short wavelengths (see comparison of the 300 K data in Fig. 6). The above difference originated mainly from transparency difference of the used substrates. As seen from Fig. 7, at T < 100 K the $D_{\lambda max}^*$ values are less than those recently published for the *InAs* DH PDs [7], however, at moderate cooling
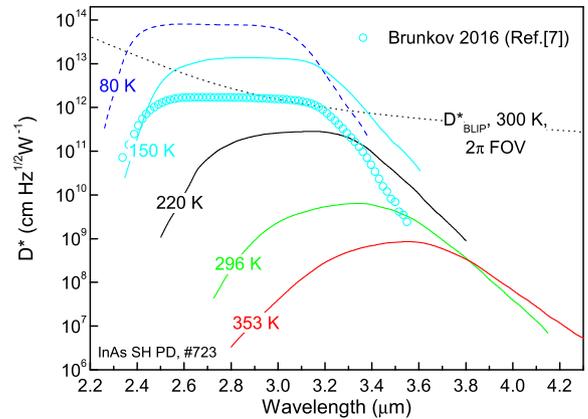
Fig. 6. Spectra of detectivity D_{λ}^* at different temperatures for single PD element. Previous data for InAs BSI DH PDs (Ref. [7], 150 K) is presented by open circles (○). Dotted line – BLIP D^* value vs wavelength (300 K ambient, 2π FOV).

Fig. 4. Zero bias resistance – area product vs temperature. In the insert – the ideality factor (β) vs temperature.
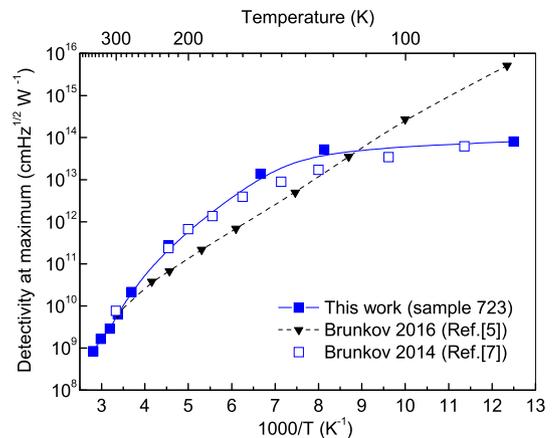
Fig. 7. $D_{\lambda max}^*$ vs temperature for single PD element (filled squares) and previous SH (open squares) and DH (filled triangles) PDs.
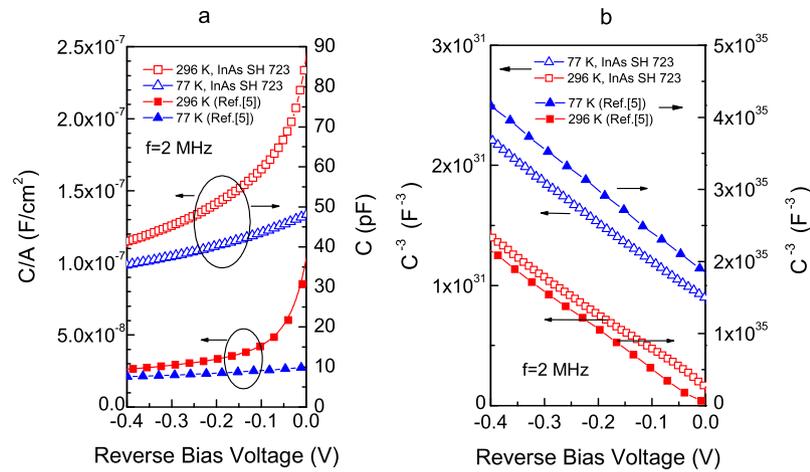
Fig. 8. C-V characteristics of single matrix element at 300 (□) and 77 (△) K (open symbols) (a), the same data in a $(1/C)^3$ presentation (b). Measurement frequency 2 MHz. Data from Ref. [5] is presented by filled symbols for 300 (▲) and 77 K (■).

(113 < T < 250 K) the ratio inverts and SH PD performance is much better than that for the single element DH PDs and is superior to previous InAs PD arrays as well. For example dark current density at 200 K in this work is about three orders lower than that reported for the 50 μm wide and large area homojunction InAs PDs in [11] and about two orders of magnitude lower than in large area InAsSbP/InAs PDs in [6]. RT $D^*_{\lambda max}$ value is of the same order as for InAs homojunction single element p-i-n PD described recently in [2] and in heterojunction PDs in [10]. The estimated BLIP operation temperature for the 2π FOV and λ_{max} = 3.1 μm amounts to 190 K which is 40 K higher than previously reported number for the DH PDs [7]. Of course, we are aware that the above temperature is a little bit exaggerated the whole matrix and not single element performance being considered. However as it follows from the histogram of the R_o distribution in Fig. 9 the mean (for all 64 elements) value is around 2.8 kΩ vs 3.5 kΩ for the element characterized in Fig. 6 and thus the estimation for abovementioned BLIP operation temperature is close to that of the matrix as well (worth noting that S values practically do not vary from element to element).

Several features of our previous *InAs* DHs and current *InAs* SHs appeared to be common. For example, capacitance of our SH PDs varied as $(1/C^3) \sim U_{bias}$ suggesting linear impurity distribution within the space charge region (see Fig. 8). As a result the fabricated PDs exhibited as low unit area capacitance as $C_o/A = 2.5 \times 10^{-7}$ and 1.3×10^{-7} F cm^{-2} at 300 and 80 K correspondingly.[2] These numbers are less than most data published on *InAs* heterostructure PDs[3] and thus one can expect small PD response time, e.g. $\tau = R_{load}C_o = 0.1$–0.45 ns for the 190 μm wide device element and standard load of R_{load} = 50 Ω.

Several experimental results in this work confirm limited influence of deep centers on transport and recombination processes. This follows e.g. from an independence of quantum yield on a forward current in a wide range of current values (see the L-I characteristic in Fig. 10) and an independence of the zero bias capacitance C_o on a modulation frequency (measured but not shown here). Indeed, the low current part of the L-I characteristic in InAs based diodes with defects exhibits usually superlinear dependence on current due to recombination via Shockley-Read centers (or "structure defects"). At high currents this type of L-I behavior is sequentially followed by linear and sublinear dependence when domination of radiative and nonradiative (Auger) recombination

respectively occurs [5]. The above competition of the three recombination mechanisms results in nonlinear dependence of quantum efficiency on current with maximum at domination of radiative recombination when output power is proportional to current [5]. As seen from Fig. 10 quantum efficiency/conversion efficiency in InAs SH already reaches it's maximum at current density as low as 0.1 A/cm^2 (region of linear dependence of intensity on current with conversion efficiency of about 0.2 mW/A). The latter current
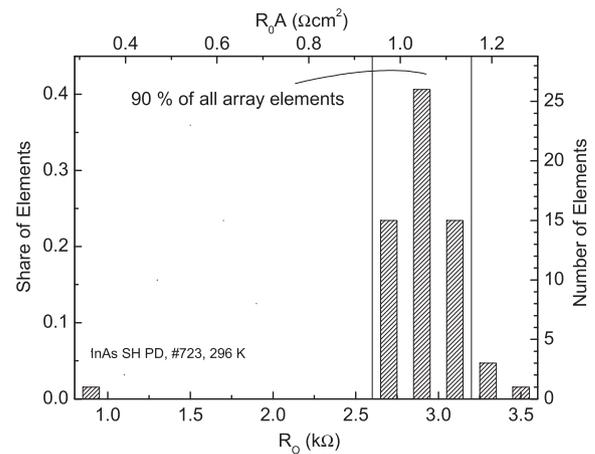
Fig. 9. Histogram of the zero bias resistance distribution in 8 × 8 PD matrix.
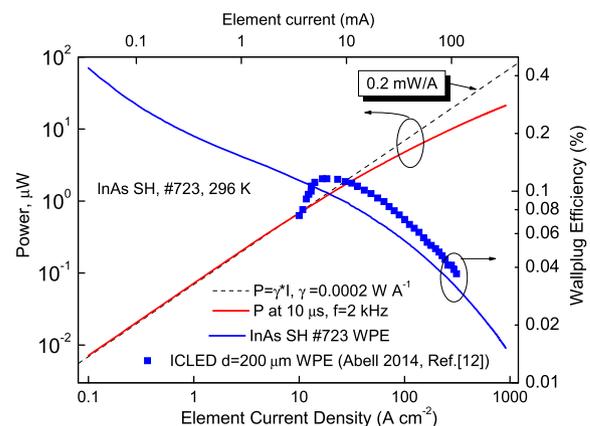
Fig. 10. L-I characteristic and WPE of a single matrix element at RT.

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[2] Capacitance data on C_o covered the 75–85 pF interval at 300 K.
[3] Typical values found in the literature are 2–4 · 10^{-7} F cm^{-2} for 77 and 300 K [6].

density value is about two orders of magnitude smaller than that for the InAs/InAsSbP DH diodes with defect density of about $(1–6) \times 10^{15}$ cm^{-3} in [5]. One can thus expect that defect density in our samples is sufficiently lower than 10^{15} cm^{-3}.

It is also worth mentioning that matrix element wallplug efficiency (WPE) (e.g. WPE = 0.1% at I = 18 A/cm^2) is fairy close to that for the recently developed "high voltage" interband cascade light emitting diodes (LED) with close spectral and dimensional characteristics (WPE$_{max}$ = 0.12% [12]). At low current density the InAs SH exhibits high WPE values that make them attractive for use as calibration source in ultra low power consumption detector systems.

An assumption on limited number of defects in our InAs SH also goes along with capacitance measurement. The stability of the $(1/C^3)$ – U$_{bias}$ slope against temperature variation confirms independence of charge carrier concentration on temperature – feature not available in semiconductor with sufficient amount of deep levels in the forbidden energy gap. The calculated concentration of charge carriers was nearly the same for 77 and 300 K; free carrier concentration in the vicinity of the p-n junction ranged from 4×10^{16} to 2×10^{17} cm^{-3}. These values appeared somewhat higher than those for the n-*InAs* DH at 300 K [7]; the latter has obviously resulted from minor deviations in DH and SH wafer growth process details.

4. Conclusion

Low dark current P-*InAsSbP*/n-*InAs*/n$^+$-*InAs* single heterostructure 8×8 photodiode array exhibited BLIP operation below 190 K (2π FOV) with negligible influence of generation-recombination and tunneling currents in the whole 150–350 K temperature interval. These features most likely arose from absence of p-InAs layer and low electrically active defect density in n-*InAs* and P-*InAsSbP* layers. Low unit area capacity (1.3×10^{-7} - F cm^{-2}, 80 K) in the above low defect density *InAsSbP/InAs* PDs with linear impurity distribution in the p-n junction makes promises for fabrication in future efficient mid-IR matrix detectors with small response time. In addition the developed large area diode array operating in the negative luminescent mode can be used for other FPA, say, CdHgTe ones, as "cold" plates that cut-off ambient/noise radiation.

Acknowledgments

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