



InAsSbP/InAs_{0.9}Sb_{0.1}/InAs DH photodiodes ($\lambda_{0.1} = 5.2 \mu\text{m}$, 300 K) operating in the 77–353 K temperature range



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ABSTRACT

Double heterostructure back-side illuminated photodiodes with a 10- μm thick InAs_{0.9}Sb_{0.1} active layer have been fabricated, studied and characterized in the 77–353 K temperature range. Spectral response peculiarities and temperature induced peak shift ($\lambda = 4\text{--}4.8 \mu\text{m}$) were explained within simple phenomenological model based on proximity of the active layer thickness and hole diffusion length while reasons for a sensitivity decrease at low temperatures are still less evident. Transition from a generation-recombination to a diffusion current flow mechanisms with temperature increase appeared to be close to that for the InAs based diodes.

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1. Introduction

In the past there have been quite sufficient number of research efforts aiming at design efficient photodiodes (PDs) with peak sensitivity at wavelengths of $\lambda_{\text{max}} = 4.6\text{--}4.8 \mu\text{m}$ (or $\lambda_{0.1} \sim 5.2 \mu\text{m}$). These PDs are important for use in low temperature pyrometry [1] as well as in nondispersive infrared (NDIR) gas analysis of carbon oxide gas that has strong absorption band near the 4.7 μm wavelength [2,3]. Together with spectrally matched light emitting diodes (LEDs) these PDs can be used for ultra low power consumption gas sensors and portable gas analyzers [2–5].

InAs_{1-x}Sb_x and In_{1-y}Ga_yAs_{1-x}Sb_x (0.1 < x < 0.15) alloys and corresponding p–n heterojunctions grown onto InAs or GaSb substrates were considered as quite traditional materials for the above PDs [6] and record zero bias resistance area product value of $R_0 A = 10^9 \Omega \text{cm}^2$ at 77 K was demonstrated in the LPE grown InAs_{0.86}Sb_{0.14}/GaSb back-side illuminated (BSI) PDs [7]. Best to date room temperature sensitivity has been reported for p-InAs_{1-x}Sb_x/InAs_{1-x}Sb_x/n-InAsSbP/n-InAs graded band gap heterostructures grown by the LPE method with peak sensitivity values ranging from $S_{I_{\text{max}}=4.7 \mu\text{m}}^{\text{max}} = 1.6 \text{ A/W}$ ($R_0 A = 0.005 \Omega \text{cm}^2$) [8] to $S_{I_{\text{max}}=4.7 \mu\text{m}}^{\text{max}} = 2.65 \text{ A/W}$ ($R_0 A = 0.0014 \Omega \text{cm}^2$) [9].

Because of high segregation coefficient at growth temperature the phosphorus concentration diminished at the surface of a 50–80 μm thick n-InAsSbP layer providing the energy gap decrease along the growth direction with $\nabla E_g = -(1\text{--}2) \text{ meV}/\mu\text{m}$ in both previously mentioned cases [8,9]. InAsSbP lattice constant at heterojunction was nearly the same as for InAs substrate ($\Delta a/a < 0.05\%$) while distant from the substrate alloy had negligible phosphorus content and was thus lattice mismatched with InAs substrate ($\Delta a/a \sim 0.5\%$). When back-side illuminated the above graded heterostructures showed relatively narrow photoresponse spectral band (FWHM < 0.7 μm) evidently due to finite diffusion length of the photogenerated holes.

For many years we believed that high $S_{I_{\text{max}}}^{\text{max}}$ values in [8,9] resulted from low threading dislocations density ($N < 10^5 \text{ cm}^{-2}$) in curved InAsSbP graded structures used for these particular PDs. Low dislocation density in [8,9] was achieved by implementing peculiar growth procedure accompanied by stress relaxation process via substrate plastic bending ($R < 10 \text{ cm}$). Data on this relaxation process (or in other words “inversion deformation process”) can be found elsewhere [10,11]. The authors of [10,11] stated that plastically deformed (bent) InAs substrate ($N_{\text{InAs}} > 10^7 \text{ cm}^{-2}$) was incorporated with the bent InAsSbP graded layer of high crystalline quality ($N_{\text{InAsSbP}} < 10^5 \text{ cm}^{-2}$). Similar data supporting general properties of the “inverse defect formation process” was traced also during the growth of GaAsSbP/GaAs [12] and InGaAsSb/InAs [13] graded heterostructures.

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On the other hand an impact of dislocation density in *InAs* substrates [14] and in *InAsSb* buffer layer [15] onto PD performance in “flat” heterostructures has been recently revealed. The authors of [15] suggested that increasing the buffer layer thickness from 1 to 9 μm resulted in sufficient dislocation density decrease that was accompanied by a 4-fold increase of the detectivity (D^*) value. The “buffer layer” approach described in [15] is evidently attractive for PD fabrication especially when growth of large format matrix PD structures (or FPA) is considered. Alternatively curved structures with “thick” *InAsSbP* or *InGaSb* buffers with $R < 50$ cm like those in [10–13,16] could hardly be integrated into large area wafer growth, photolithography and assembling procedures.

Additional motives for investigation *InAsSb* based PDs include a desire to improve electrical design of PD chip that could enhance device performance. Most known *InAsSbP* PDs with $\lambda_{\max} = 4.6\text{--}4.8$ μm suffer from poor collection efficiency of photo-generated carriers that originate from current crowding effects in front surface illuminated (FSI) structures with small area anodes formed onto low conductivity cladding [17] or substrate [16]. As a result most FSI PDs exhibit low sensitivity with a typical value of $S_{I,300K}^{\max} = 0.2\text{--}0.3$ A/W (see, e.g. [18]). Let us also note that relatively high R_oA product values in many published FSI PDs originated from the abovementioned current crowding effect. Electrically active area in such PDs approximately amounted to that of the anode area [17].

Although the *InAsSb* bariode structures with background-limited performance (BLIP) at 160 K were already used for matrix fabrication [19] they need sufficient bias for operation. Alternatively conventional *InAsSb* double heterostructure (DH) *p-n* structures can operate in a photovoltaic mode, however no recent investigations at low temperatures ($T < 250$ K) have been undertaken.

Here we present data on wide temperature range performance of 4.7 μm BSI PDs fabricated from “flat” (curvature radii > 50 cm) *n-InAs/n-InAsSb/p-InAsSbP* DH with broad reflective anode formed onto *p-InAsSbP* surface.

2. Experimental details

LPE grown heterostructures consisted of *n*-type *InAs*(100) substrates with $n = 2 \cdot 10^{16} \text{ cm}^{-3}$ (for undoped) or $n^+ = 2 \cdot 10^{18} \text{ cm}^{-3}$ (for the *Sn* doped) substrates, ~ 10 μm thick undoped *n-InAs_{1-x-y}Sb_x* active (absorbing) layers and finally *p-InAs_{1-x-y}Sb_xP_y(Zn)* claddings (contact layer) (see Fig. 1). As seen from Fig. 1 the narrow gap *InAsSb* active layer was surrounded by semiconductors with wider energy gap. The energy gap difference at heterojunction was bigger

than doubled thermal energy ($\Delta E_g > 2kT$, k – is the Boltzman constant, T – temperature) which justifies the use of the term “double heterostructure” (DH) in the paper title.

Photoluminescence (PL) spectra measured at a temperature of $T_1 = 77$ K in a “reflection geometry”, that is, from the *p-InAs_{1-x-y}Sb_xP_y* side exhibited two overlapping emission bands with peaks at $h\nu_{InAsSbP}^{77K} \approx 357$ meV (evidently originating from *InAsSbP* quaternary emission) and $h\nu_{InAsSb}^{77K} \approx 310$ meV (coming from the narrow band *InAsSb* ternary) respectively (see Fig. 2). We believe that no nonequilibrium emission came from the n^+ -*InAs* substrate because of relatively big *InAsSb* layer thickness (absorption). PL peak difference constituted to $\Delta h\nu^{77K} = h\nu_{InAsSbP}^{77K} - h\nu_{InAsSb}^{77K} = 47$ meV which correlated with the interpolated energy gap difference at the 2-nd heterojunction where $\Delta E_g^{77K}(x,y) = E_g(x_1,y_1) - E_g(x_2,y_2) = 390 - 335 = 55$ meV. The expected PL peak energy for the *InAsSb* alloy at $T_2 = 300$ K is close to $h\nu_{InAsSb}^{300K} = h\nu_{InAsSb}^{77K} - \Delta E_g^{77-300K} + k(T_2 - T_1)/2 = 270$ meV temperature variation of the energy gap being the same as for the *InAs* binary ($\Delta E_g^{77-300K} = 55$ meV [20,21]). The expected *InAsSb* PL peak energy $h\nu_{InAsSb}^{300K}$ is in good agreement with the electroluminescence peak (EL) value of 263 meV measured at 296 K in a transmission mode (see the insert in Fig. 2). We didn't analyze agreement between PL and EL spectra at 77 K as the measurements were carried out in the presence of normal atmosphere (0.03 v/v% of CO_2 , total optical path of ~ 2 m) and both spectra were distorted by the CO_2 gas absorption at 4.3 μm. As seen from the graph in Fig. 2 there was no shortwave EL radiation coming from the broad band gap *p-InAsSbP* layer evidently due to efficient absorption in the *InAsSb* narrow gap layer.

Standard optical photolithography and wet chemical etching processes developed by Ioffe Institute together with IoffeLED, Ltd. have been implemented to obtain 26 μm high circular mesas ($\varnothing_m = 190$ μm) and 55 μm deep grooves for separation of the 580×430 μm rectangular chips. Circular *Au*- or *Ag*-based reflective anode ($\varnothing_a = 170$ μm) and cathode contacts were formed on the same chip side by sputtering and thermal evaporation in vacuum followed by thick (3 μm) gold plating deposition as described elsewhere [22,23]. Preliminary evaluation showed no radical difference between reflection properties in the above contact types. Flip-chip bonding/packaging procedure has been implemented using the 1800×900 μm submount made from semiinsulating *Si* wafer with *Pb-Sn* bonding pads. PD chips were mounted up-side down, n^+ -*InAs* side being an “entrance window” for the incoming

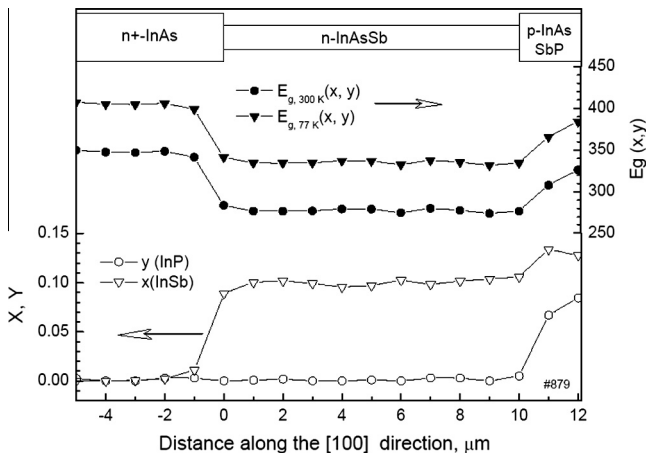


Fig. 1. Alloy composition and simulated values of the energy gap vs distance from the 1-st *InAs/InAsSb* heterojunction.

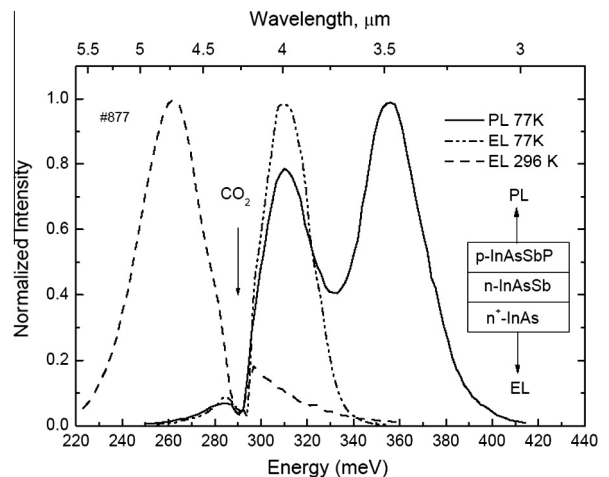


Fig. 2. Electro- and “reflection” photoluminescence spectra in *InAsSb* DH PD at 77 and 300 K.

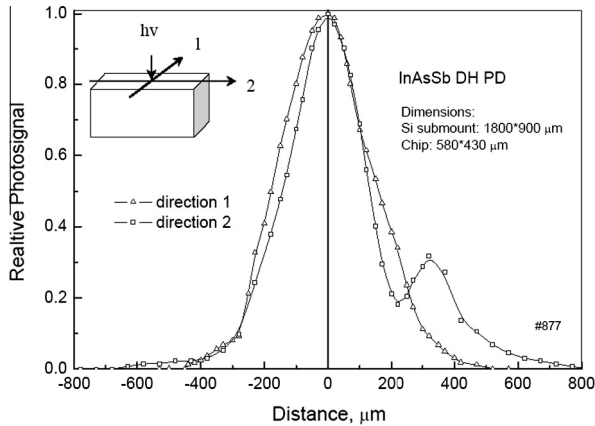


Fig. 3. Distribution of the photosignal along two orthogonal directions (1 and 2) intersecting the mesa center projection onto n^+ -InAs surface in bare chip PD.

radiation as shown in the insert in Fig. 7. TO-18 standard case was chosen for bare chip PDs package while some chips were equipped with aplanatic hyperhemispherical Si immersion lenses ($\varnothing = 3.5$ mm) with antireflection coating using a chalcogenide glass as an optical glue between Si and n^+ -InAs (or n -InAs) as described elsewhere [1,3–6,8].

As seen from Fig. 3 bare PD chips exhibited broad spatial sensitivity suggesting that an optical area was sufficiently larger than the mesa one. Having in mind abovementioned enhanced optical collection ability we undertook sensitivity measurements using circular diaphragm ($\varnothing = 100$ μm) placed in front of the n^+ -InAs (or n -InAs) PD “face” just above the center of the active area as shown in the insert in Fig. 7. The diaphragm shadowed photon fluxes outside mesa area and thus the input optical power were governed by a 573 K black body (BB) power and a distance between the BB and PD. There was no need to use diaphragm for the immersion lens PD characterization; optical area was considered equal to an open lens part, that is, to a circular area of $0.25 \cdot \pi \cdot (3.2 \text{ mm})^2$. The assumption is true if all radiation beams that hit lens surface enter PD active area. Spectral response measurements were performed using a Globar as a light source.

I - V characteristics were measured at $I = 10^{-12}$ – $2 \cdot 10^{-3}$ A under dark conditions at the CW mode using the sub-femtoampere SourceMeter Keithley 6430 equipped with remote preamplifier. Due to mechanical reasons originated from temperature expansion coefficient mismatch in the immersion lens package the I - V as well as the responsivity measurements were performed using two different package options. In fact the immersion lens PDs were used for the I - V and sensitivity measurements in the $-20 \dots +80$ °C temperature range whereas unprotected/bare PD chips mounted onto TO-18 case were used for their characterization at low temperatures ($77 < T < 280$ K).

3. Results and discussion

In Fig. 4 one can find typical I - V characteristics together with the $I = I_0 \cdot \exp(eV/\beta kT)$ function presented by straight dashed lines. Good matching of the above exponent and the forward bias (FB) I - V curves for $T < 220$ K is evident. “High temperature” ($T > 220$ K) I - V data has poor matching with exponents at high currents probably due to series resistance impact. On the other hand current leakage at a reverse bias (RB) is progressively decreasing as temperature grows leading to nearly ideal Shockley I - V characteristics near room temperature with current saturation at high RB. The same conclusion comes from analysis of the β and I_0 temperature dependences shown in Fig. 5. As seen from Fig. 5 the ideality

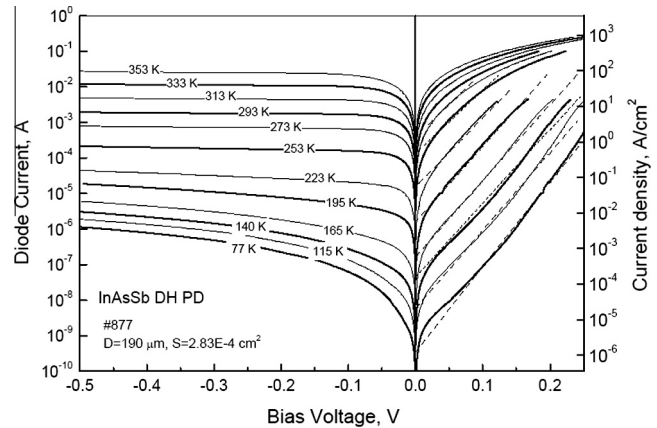


Fig. 4. Bare chip and immersion lens PD I - V characteristics at several temperatures. Straight dashed lines in the forward bias region correspond to the modified Shockley formula.

factor β approaches unity at 300 K and approaches 2 at ~ 110 K suggesting transition from diffusion (at high T) to generation–recombination (at low T) current flow mechanism. Low temperature data ($T = 77$ K) evidently suggests domination of the tunneling mechanism as $\beta \rightarrow 3$.

The above transformation of the current flow mechanism can be also traced from the Arrhenius plot in Fig. 6 with where temperature dependence of zero bias resistance (defined as $R_0^{U=0}$ and $R_0^{U>0}$) is presented. The $R_0^{U=0}$ values were extracted from low bias measurements ($|U| < 0.005$ V), while the $R_0^{U>0}$ values were understood as $R_0^{U>0} = \beta kT/eI_0$, where I_0 – is the zero bias current – parameter derived from interpolation. As seen from Fig. 6 both $R_0^{U=0}$ and $R_0^{U>0}$ values exponentially grow on temperature decrease, whereas growth rate is sufficiently different at low and high temperatures. The energy parameter E in the above exponent ($\exp(-E/kT)$) for both R_0 values is fairly close to InAsSb energy gap value ($E = 0.3$ eV) which confirms diffusion current domination at least in the 200–350 K temperature interval. At low temperatures the $R_0^{U=0}$ and $R_0^{U>0}$ values split as additional leakage takes place (see deviation from ideal I - V characteristic at small forward bias in Fig. 4). Meanwhile a guess that generation–recombination current dominates at low temperatures ($\beta = 2$) is true for fairly small temperature interval as seen from comparison of low temperature

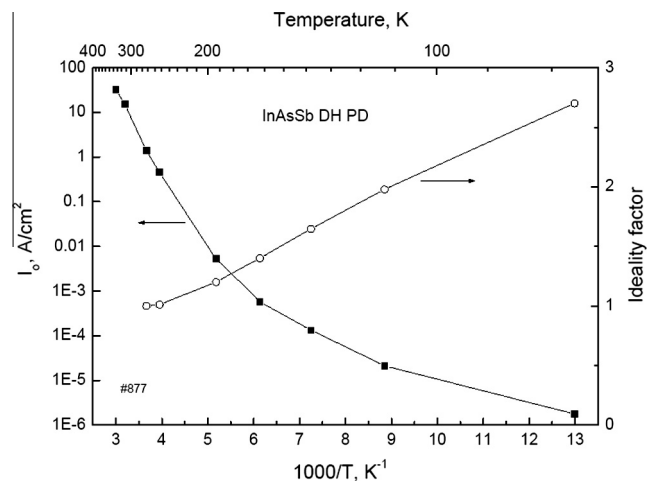


Fig. 5. Saturation current (I_0) and ideality factor (β) values derived from the forward bias data.

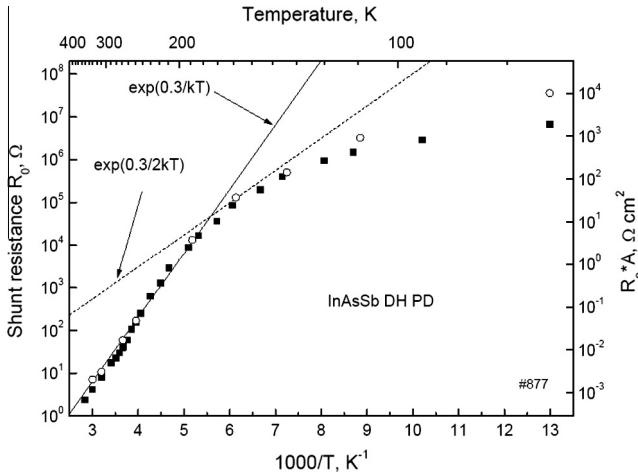


Fig. 6. Temperature dependence of the zero bias resistance derived from direct measurement at $|U| < 0.005$ V (filled squares) and from the I_0 values shown (open symbols). Straight lines correspond to $\exp(0.3/kT)$ and $\exp(0.3/2kT)$ functions.

data and the $\exp(-E/2kT)$ function. The above transition from diffusion to generation–recombination current flow mechanisms and transition temperature value do not conflict with the known features of InAs like diodes (see e.g. [6,7]) including our own observations in p -InAsSbP/ n -InAs/ n^+ -InAs PDs [24]. At low temperatures tunneling seems to prevail – a confirmation for this are high β values (Fig. 5) and slow R_0 growth (Fig. 6).

Shown in Figs. 7 and 8 are the spectral response and detectivity at different temperatures measured in bare chip PDs equipped with diaphragm (see Section 1) and in immersion lens PDs containing “natural diaphragm” formed by a 3.2 mm wide open lens part. Within measurement accuracy ($\pm 5\%$) sensitivities in bare chip and immersion lens PDs have similar numbers at least in the $t = (-20)$ – (40) °C temperature range. Proximity of above values confirms good collimation of radiation beams in immersion lens PDs.

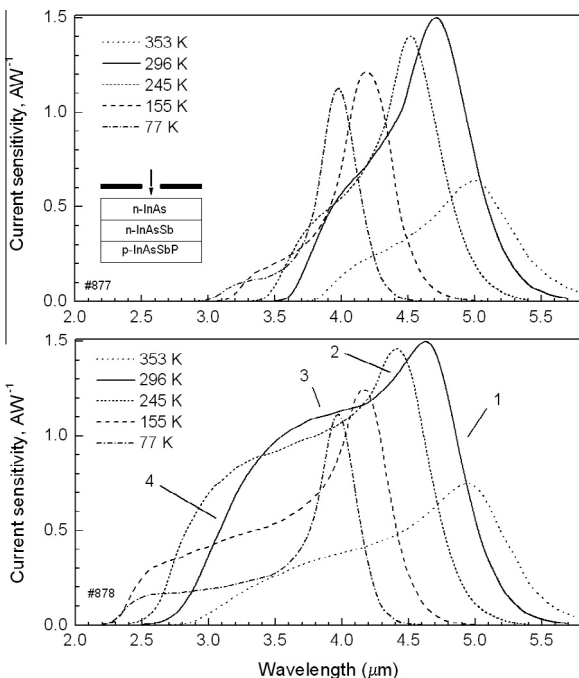


Fig. 7. Response spectra in n -InAs (upper graph) and n^+ -InAs (bottom graph) based PDs with InAsSb absorbing layer at 77, 155, 245, 296 and 353 K.

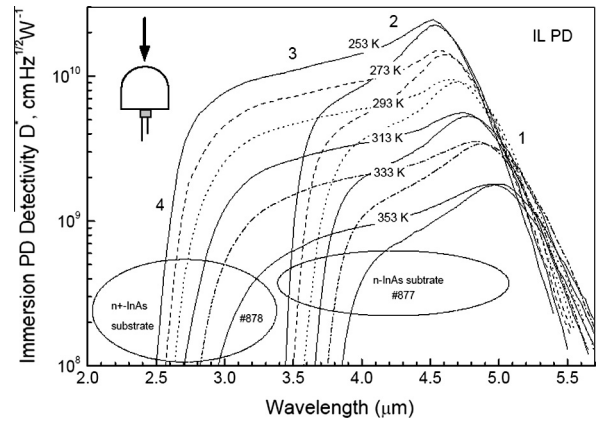


Fig. 8. Detectivity spectra in n -InAs and n^+ -InAs based PDs with InAsSb absorbing layer at $-20, 0, 20, 40, 60$ and 80 °C.

As seen from Figs. 7 and 8 the responsivity spectra bears four distinct regions: the cut-off region ($4.7 < \lambda < 5.5$ μm) (1), sharp longwave response decline region (2), smooth response decline region (3) and finally fast shortwave response decline region (4). The latter region is evidently due to transmission degradation in heavily doped n^+ -InAs substrate with degeneration of electrons in the conduction band. In our case the Moss-Burstein associated absorption edge shift in n^+ -InAs is as large as 1 μm (compare data for PD with heavily doped (#878 sample) and undoped (#877 sample) substrates in Fig. 7).

Sharp response decline in region 2 (in Fig. 7) is a consequence of the absorption coefficient increase and corresponding decrease of the number of photogenerated electron-hole pairs in a vicinity of a p - n junction. We assume that the hole diffusion length (L_{diff}) is of the same order or larger than the InAsSb thickness and thus subsequent absorption coefficient increase (at a wavelength decrease – region 3) leads to more or less stable portion of carriers that can reach p - n junction by diffusion. Large absorption means that the majority of photons are absorbed near the n (n^+)-InAs/ n -InAsSb interface, that is, at fixed distance from the p - n junction. The latter assumption nicely meets our previous estimations of L_{diff} in InAsSbP graded band gap PDs with InAsSb active zone [8]. Proximity of layer thickness d and L_{diff} values could explain broad spectral response in our BSI PDs. Alternatively in BSI PDs based on thick graded heterostructures with $d \gg L_{diff}$ photoresponse is narrow due to large distance for hole traveling from broad band InAsSbP absorbing region to the p - n junction.

It is worth mentioning that there is no 100% coincidence of the spectra shape in region (2) and (3) for the PDs grown onto n -InAs and n^+ -InAs substrates. At the moment we are not able to erect the verdict “who is guilty” for that discrepancy but are willing to get knowledge on that in our future work.

Fig. 7 states that PDs response reaches its maximum at temperatures close to 300 K and degrades at elevated and low temperatures. Sensitivity degradation for PDs with “entrance window” made from heavily doped n^+ -InAs at elevated temperatures was already explained by substrate transmission changes [6,8], while reasons for sensitivity degradation at low temperatures and in PDs with n -InAs substrate are still unclear. The above degradation at low temperatures could be explained by a diffusion length decrease in InAsSb. However, there is no strong experimental evidence for that so far save data in [7] where statement of $L_{diff} = 5.5$ μm at 77 K for the BSI PDs has been made.

Superposition of R_0 (Fig. 6), S_I (Fig. 7) values and Johnson detectivity formula ($D^* = S_I(R_0 A_{p-n}/4kT)^{0.5}$) provides $D_{\lambda, \text{max}}^*$ values shown in Figs. 8 and 9. Temperature variation of sensitivity and peak

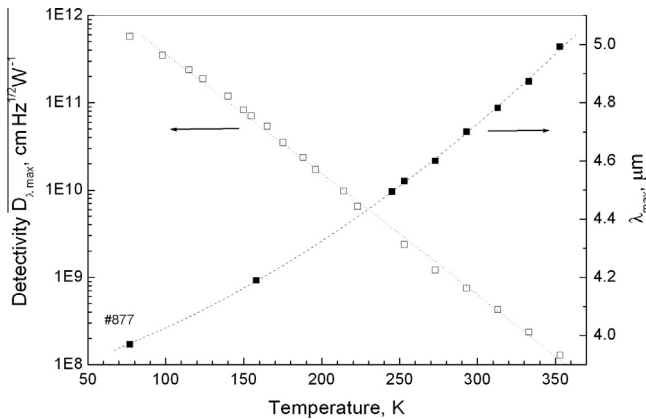


Fig. 9. Detectivity at maximum and peak wavelength vs temperature in *n*-InAs based bare chip PD with InAsSb absorbing layer.

position were taken into account using graphs in Figs. 7 and 10. In all simulations including internal quantum efficiency calculation the A_{p-n} number (the *p*-*n* junction area) was substituted by the mesa area value. For the immersion lens PDs the $D_{\lambda,max}^*$ values are generally about decade higher than those for bare chip PDs [8]; the same tendency was confirmed in our current measurements (see Fig. 8).

As seen from Fig. 9 the developed PDs are not superior to those in [15] at room temperature but exhibit better $D_{\lambda,max}^*$ values than published ones for InAsSb/InAs DH [18,25] or GaSb/InGaAsSb type II heterostructure PDs [26]. Moreover PDs in this study are characterized by higher internal quantum efficiency/current sensitivity (see Figs. 7 and 10) than all abovementioned PDs save the “old ones” in [9]. At low temperature the developed PDs remain “quantum efficient” while the simulated $D_{\lambda,max}^*$ values are higher than that for the graded band gap PDs [27] and fairly close to those displayed by InAs_{0.85}Sb_{0.15}/InAs_{1-x}Sb_x/InAs/GaAs [28] and InAsSb/GaSb lattice matched heterostructure PDs [29]. However former PDs have several times smaller R_0A value; in the latter case as well in [19] the PDs need electrical bias for appropriate operation – a feature that creates certain difficulties in some kind of applications. At the same time we were not able to achieve the R_0A product as high as in [7]; PDs in [7] are still champions among all 4 μm PDs known to us.

The simulated $D_{\lambda,max}^*$ values in our bare chip PDs at 77 K are close to the 2π BLIP numbers defined in [30] for the 300 K environment. Our future work will be concentrated on noise measurements to confirm high InAs/InAs_{0.9}Sb_{0.1}/InAsSbP DH PD performance at low temperatures.

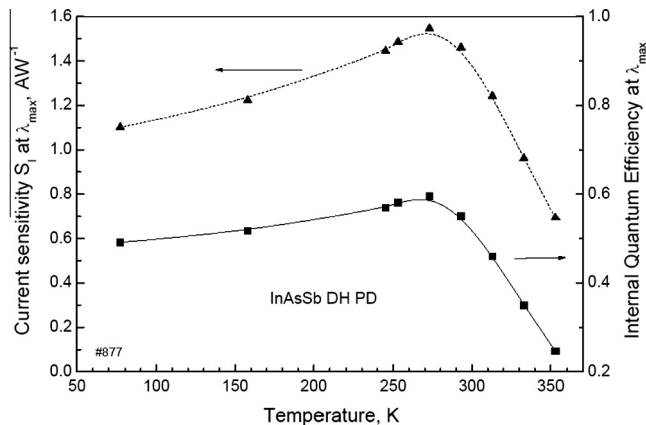


Fig. 10. Peak sensitivity and internal quantum efficiency vs temperature in *n*-InAs based bare chip PD with InAsSb absorbing layer.

4. Conclusion

Broad band DH BSI PDs with 0.19 mm wide active layers made from InAs_{0.9}Sb_{0.1} grown onto *n*-InAs or *n*⁺-InAs substrates showed diffusion current flow and negligible leakage current flow mechanisms at $T > 190$ K, while at lower temperatures generation–recombination at high bias and tunneling at low bias prevail. Internal quantum efficiency peaked at 270 K ($\eta = 0.6$) and appeared higher than in many close analogues with the result that the bare chip current sensitivity and simulated detectivity reached values acceptable for many applications: $S_{\lambda,max}^* = (0.6–1.5)A/W$, $D_{4.7\mu m}^* = 8 \cdot 10^8$ and $D_{4.0\mu m}^* = 6 \cdot 10^{11}$ cm Hz^{1/2} W⁻¹ at 300 and 77 K correspondingly. Immersion lens PD options ($\emptyset_{open\ area} = 3.2$ mm) offer similar $S_{\lambda,max}^*$ and a decade higher D^* values.

Conflict of interest

There is no conflict of interest.

Acknowledgments

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